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# **sta-constraint-validator Documentation**

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CHAPTER  
**ONE**

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**PROCESS**



## BOARD DATA

The board data data structure contains all the information about trace delays. It has the following basic structure:

```
board:
  trace:
    - <trace_name>:
      device_pin: <pin_name>
      part_pin: <pin_name>
      delay:
        max: <max_delay>
        min: <min_delay>
```

Element	Type	Description
trace_name	string	The name of the trace on the board.
pin_name	string	Name of the pin on the device or part the trace connects to.
max_delay	float	The maximum delay of the trace.
min_delay	float	The minimum delay of the trace.

### 2.1 Example

The following example will illustrate how to fill out the data structure.

The above image would result in the following YAML file:

```
board:
  trace:
    - read_data:
      device_pin: 'E'
      part_pin: 'F'
      delay:
        max: 1.0
        min: 0.5
    - write_data:
      device_pin: 'C'
      part_pin: 'D'
      delay:
        max: 1.0
        min: 0.5
    - clock:
      device_pin: 'A'
```

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```
part_pin : 'B'  
delay:  
  max: 1.0  
  min: 0.5
```

## DEVICE

The device is the FPGA or ASIC which contains your design.

```
device:
  vendor: <vendor_name>
  name: <part_name>
  interface:
    - <interface_name>:
      clock:
        internal:
          - <internal_clock_name>:
              frequency: <clock_frequency>
        input:
          - <clock_pin_name>
              frequency: <clock_frequency>
        output:
          - <clock_pin_name>
              frequency: <clock_frequency>
      data:
        output:
          - <output_pin_name>:
              launch_clock:
                name: <launching_clock_name>
                edge: <launching_clock_edge>
              capture_clock:
                name: <capturing_clock_name>
                edge:
                  setup: <capturing_clock_edge>
                  hold: <capturing_clock_edge>
        input:
          - <input_pin_name>:
              launch_clock:
                name: <launching_clock_name>
                edge: <launching_clock_edge>
              capture_clock:
                name: <capturing_clock_name>
                edge:
                  setup: <capturing_clock_edge>
                  hold: <capturing_clock_edge>
```

Element	Type	Description
vendor_name	string	The manufacturer of the part.
part_name	string	The name of the part.
interface_name	string	Devices can have multiple interfaces. Each must be uniquely identified.
internal_clock_name	string	The internal clock name being used to launch or capture data.
clock_frequency	string	The frequency of the clock.
clock_pin_name	string	The clock pin the data pins are referenced to.
output_pin_name	string	Each output pin will have an entry.
launching_clock_edge	integer	The clock edge which is launching data.
capturing_clock_edge	integer	The clock edge which is capturing data.
clock_to_out_min	float	The minimum delay of the pin relative to the clock pin.
input_pin_name	string	Each input pin will have an entry.

### 3.1 Example

The following example assumes using the serial interface of the DAC81404 part.

```
part:
  vendor: Intel
  name: S10
  interface:
    - DAC_DATA_INTF:
      clock:
        internal:
          internal_100mhz:
            frequency: '100 MHz'
      output:
        O_DAC_SCLK:
          frequency: '20 MHz'
      data:
        output:
          - O_DAC_DATA:
            launch_clock:
              name: 'internal_100mhz'
              edge: 11
            capture_clock:
              name: 'O_DAC_SCLK'
              edge:
                setup: 'c'
                hold: 'd'
        input:
          - I_DAC_DATA:
            launch_clock:
              name: 'O_DAC_SCLK'
              edge: 3
            capture_clock:
              name: 'internal_100mhz'
              edge:
                setup: 'f'
                hold: 'q'
```

The part is the external device the FPGA/ASIC is communicating with. It is typically provided by a vendor.

```
part:
  vendor: <vendor_name>
  name: <part_name>
  interface:
    - <interface_name>:
      timing_model : <interface_type>
      clock:
        input:
          - <clock_pin_name>:
              max_freq: <frequency>
        output:
          - <clock_pin_name>:
              max_freq: <frequency>
      data:
        input:
          - <input_pin_name>:
              clock: <clock_name>
              <clock_edge>:
                setup:
                  id: <timing_id>
                  value: <setup_value>
                hold:
                  id: <timing_id>
                  value: <hold_value>
        output:
          - <output_pin_name>:
              clock: <clock_name>
              <clock_edge>:
                clock_to_out_max:
                  id: <timing_id>
                  value: <clock_to_out_max>
                clock_to_out_min:
                  id: <timing_id>
                  min: <clock_to_out_min>
```

## 4.1 Example

The following example uses a Texas Instruments DAC81404 part.

```
part:
  vendor: Texas Instruments
  name: DAC81404
  interface:
    - serial_interface:
      timing_model : 'source synchronous with round trip'
      clock:
        SCLK:
          max_freq: '50 MHz'
      data:
        - SDIN:
          falling_edge:
            setup:
              id: 'tSDIS'
              value: '5 ns'
            hold:
              id: 'tSDIH'
              value: '5 ns'
        - SYNC_F:
          falling_edge:
            setup:
              id: 'tCSS'
              value: '20 ns'
            hold:
              id: 'tCSH'
              value: '5 ns'
        - SDO:
          rising_edge:
            clock_to_out:
              name: 'tSDODLY'
              max: '20 ns'
              min: '0 ns'
```

## INDICES AND TABLES

- genindex
- modindex
- search